

Design and Simulation of Partial SDR Platform¹

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Abstract

Software Defined Radios (SDR) are highly configurable hardware and software platforms that enable the implementation of the rapidly expanding 3G and 4G digital wireless communication infrastructures. Many sophisticated signal processing tasks are performed in a SDR platform, for example: channel estimation, equalisation, forward error correction, adaptive antennas, rake receiving, modulation, advanced compression algorithms, and vocoding. The research program (proposed by the author and approved by the university of Damascus and the university of Portsmouth-UK) suggested the following steps:

- 1-Literature survey of GSM and CDMA communication systems
- 2-Software Defined Radio (SDR) principles and technologies with more emphasis on the baseband processing
- 3-Partial design and simulation of selected parts of SDR platform, keeping in mind the possibility of reconfiguring the platform to work as GSM or CDMA system

An expanded literature survey has been achieved during the first part of the sabbatical leave at the University of Portsmouth (ECE). The outcome of this stage (steps 1&2) was reported in the internal report 05/10 issued by the ECE on November 2005; while the results are submitted to the ICTTA-06 conference to be held in Damascus on April 2006.

Basing on the results of steps 1 and 2, we suggest a conceptual design of a SDR platform that can be reconfigured to any one of the most deployed air interfaces standards mainly: UTRA-FDD (3G standard), GSM and IS-136 (2G standard) as well as GPRS/EDGE standard (2.5G standard). Adaptability and standard parameterisation were adopted to achieve this step in order to assure the functionality of the different signal processing required to each mode of operation.

¹ For the paper in Arabic see pages (73-74).

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A generalized modulator design and simulation have been suggested as a basic part of the SDR platform and the most important part in this stage of our work. The complete platform adopts the FPGA and DSP technologies via three postgraduate projects (in ECE-Portsmouth). Virtex-11 (XC2VP20) from Xilinx and TMS320C60x DSP from TI are our choice for the implementation. Trans-programs design tools (Matlab, Simulink, RTL, VHDL, Assembly) were strongly demanded to achieve the complete platform's design and optimization.

Several design problems, related to different standard's parameters, were successfully solved and the results were included in Table 8. These are related to the reconfiguration process of the general modulator from UTRA-FDD to GSM, IS-136 and EDGE. This is achieved by the Matlab simulation, which also confirms the fact that UTRA-FDD standard requires much more computation power than the other standards. As for the receiver part, more elaboration and simulation work are required. The coordination between the team work at ECE and the author will continue in order to achieve this fundamental part successfully. The results will be reported later in accordance with the progress achieved of this research work.

1- Introduction

Software Defined Radios (SDR) are highly configurable hardware and software platforms enabling the implementation of the rapidly expanding 3G and 4G digital wireless communication infrastructures. Many sophisticated signal processing tasks are performed in a SDR, for example: channel estimation, equalisation, forward error correction, adaptive antennas, rake receiving, modulation, advanced compression algorithms and vocoding [1].

2- Enabling Digital Devices And Sub-Systems

Traditionally, wireless infrastructure radio designs have been implemented using a combination of Application Specific ICs (ASICs), Digital Signal Processors (DSPs) and Field Programmable Gate Array (FPGA) devices. In these designs ASICs and FPGA handle advanced coding schemes, such as Reed Solomon, Viterbi and rake receive, while DSP have been tasked with handling coding and other tasks. SDR designers now spend considerable effort evaluating better choices of implementation due to the performance enhancement related to each option [2,3].

The wireless network infrastructure is also undergoing several changes since the old 1G systems. Table 1 depicts the different standard of mobile communication in Japan, US and Europe, while Figure(1) indicates the processing requirements for the actual standards and systems with prediction to those needed for the future 4th and 5th generations [4].

Japan	PDC and PHS	TIA/EIA-95B	Cdma-2000 + WCDMA + GPS + Bluetooth +802.11
US	TIA/EIA-136 GSM, TI/EIA-95 AMP	TIA-EIA-136 GSM/GPRS; EDGE	(Cdma-2000) WCDMA + GPS + Bluetooth + 802.11
Europe	GSM	GSM-HSCSD; GSM/GPRS, EDGE	WCDMA + GPS + Bluetooth + 802.11

Table 1: Current Wireless Standards

Each of the new higher speed services is meant to deliver advanced applications, such as MPEG-4 streaming video, two-way video, advanced location services and interactive gaming. Clearly, it is difficult to make the transition quickly to new network technologies when millions of

wireless customers already have devices that are not upgradeable to new standards.

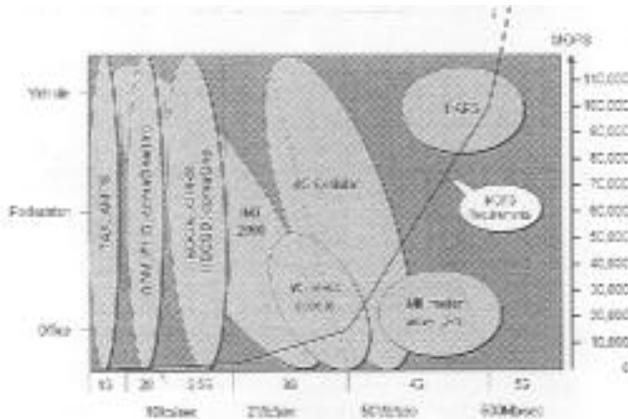


Figure 1: Processing Requirements of Wireless Systems

3- Adaptability And Standards Parameterization

For a software defined radio (SDR), adaptability means that the radio is able to process signals of different mobile standards.

Software download is a procedure by which the software relating to a specific standard may be downloaded to the hardware of the radio. Error free download can be guaranteed much more easily if it is done by smart card than over the air. One way to circumvent the drawbacks of software download, over the air, is the parameterization of standards [4].

The final goal of adaptability will be the definition of a radio knowledge representation language (RKRL), by which only a service that has to be supported by the radio has to be specified. From toolbox of mod/demodulator, as well as transmit/receive protocols, a transceiver is constructed and also the optimal signal processing and **Quality of Service (QoS)** are chosen.

3-1 GSM Air-Interface

Global System for Mobile communication (GSM) was introduced as a radio standard in Europe in 1990. the most important parameters of the GSM interface are outlined in Table 2.

Uplink	890-915 MHz (1710-1785 MHz)
Downlink	935-960 MHz (1805-1880 MHz)
Channel width	200 kHz
Channel access	FDMA/TDMA
Duplex mode	FDD/TDD
Duplex distance	45 MHz/1.73 ms (95 MHz/1.73 ms)
Users per carrier frequency	8
Speech encoder	RPE-LTP
Net speech rate	13 kbit/sec
Modulation	GMSK (BT = 0.3)
Error correcting coding	CRC, convolutional
Number of carrier frequencies	124 (374)
Bit duration	3.692 microsecond
Number of bits per time slot	156.25
Burst duration	576.9 microsecond
Channel bit rate	270.833 kbit/sec
Maximum cell radius	35 km (10 km)

Data in parentheses refer to GSM 1800

RPE-LTP: Regular Pulse Excited-Long Term Prediction

Table 2: Key air interface parameters of GSM

3-2 IS-136 Digital Advanced Mobile Phone Service (DAMPS)

IS-136 is the North American equivalent of GSM. Table 3 summarised the most important features of the **Time Division Multiple Access - TDMA** standard.

Uplink	824-849 MHz
Downlink	869-894 MHz
Channel width	30 kHz
Channel access	FDMA/TDMA
Duplex mode	FDD/TDD
Users per carrier frequency	3
Speech encoder	VSELP
Net speech rate	7.95 kbit/sec
Modulation	$\pi/4$-DQPSK
Error correcting coding	CRC, convolutional
Number of carrier frequencies	832
Bit duration	20.57 microsecond
Number of bits per time slot	324 bit
Burst duration	6.67 milisecond
Channel bit rate	48.6 kbit/sec
Maximum cell radius	20 km

Table 3: Key air interface parameters of IS-136

3-3 Ultra-Fdd Air- Interface

The European version of the third generation standard: Universal Mobile Telecommunication System (UMTS) provides two interfaces; UTRA-FDD and UTRA-TDD. The two air interfaces share several similarities: The later requires synchronization in the down – as well as the uplink while the former uses different frequency bands for up and downlink as well as higher spreading factors [4].

The cell radius of UMTS Terrestrial Radio Access Frequency Division Duplex (UTRA-FDD) is bigger and the users can move at higher velocities compared with UMTS Terrestrial Radio Access Time Division Duplex (UTRA-TDD). Table 4 illustrates the most important parameters of the UTRA-FDD standard.

Access mode	Direct sequence (DS) CDMA
Duplex mode	FDD
Chip rate	3.48 Mchip/sec
Net data rate	8 kbit/sec to 2 Mbit/sec
Spreading sequences	OVSF codes
Spreading factor	2^k ($k = 2,3,\dots,8$); 512 for downlink only
Bandwidth	5 MHz
Channel coding	Convolutional, turbo, CRC codes, interleaving
Modulation mode	QPSK
Chip impulse shaping factor	Root raised cosine, roll-off factor 0.22
Power control	Two closed and one open loop, up and downlink
Specific properties	Orthogonal spreading sequences for variable SF
Frame duration	10 ms
Slot duration	0.667 ms
Number of slots per frame	15

Table 4: Key Air Interface Parameters of UTRA-FDD

3-4 EDGE/GPRS Air- Interface

EDGE (Enhanced Data rate for GSM Evolution) is the next step in the evolution of GSM and IS- 136. The objective of this technology is to increase data transmission rates and spectrum efficiency and to facilitate new applications and increased capacity for mobile use. With the introduction of EDGE in GSM phase 2+, existing services such as GPRS

(General Packet Radio Service) and high-speed circuit switched data (HSCSD) are enhanced by offering a new physical layer. The services themselves are not modified. EDGE is introduced within existing specifications and descriptions rather than by creating new ones[5]. Basically, EDGE only introduces a new modulation technique and new channel coding that can be used to transmit both packet-switched and circuit-switched voice and data services. EDGE is therefore an add-on to GPRS and cannot work alone. GPRS has a greater impact on the GSM system than EDGE has. By adding the new modulation and coding to GPRS and by making adjustments to the radio link protocols, EGPRS (Enhanced GPRS) offers significantly higher throughput and capacity. The 8PSK modulation method used for EGPRS- MCS5 to MCS9 (Modulation Coding Scheme 5 to 9) increases the total data rate by a factor of three. Table 5 indicates the most important parameters of EDGE standard.

Uplink	890-915 MHz (1710-1785 MHz)
Downlink	935-960 MHz (1805-1880 MHz)
Channel width	200 kHz
Channel access	FDMA/TDMA
Duplex mode	FDD/TDD
Duplex distance	45 MHz/1.73 ms (95 MHz/1.73 ms)
Users per carrier frequency	8
Speech encoder	RPE-LTP
Net speech rate	13 kbit/sec
Modulation/Coding	GMSK/ for MCS1,MCS2,MCS3,MCS4 8PSK/ for MCS5,MCS,6,MCS7,MCS8,MCS9
Error correcting coding	CRC, convolutional
Number of carrier frequencies	124 (374)
Bit duration	1.23 microsecond
Number of bits per time slot	468.75
Burst duration	576.9 microsecond
Channel bit rate	812.49 kbit/sec
Maximum cell radius	35 km (10 km)

Data in parentheses refer to GSM 1800

RPE-LTP: Regular Pulse Excited-Long Term Prediction

Table 5: Key air interface parameters of EDGE

4- Proposed Software Radio (Sdr) Implementation

The design, simulation, and implementation of SDR transceivers are commonly considered as a huge and challenging task. In our case, we suggest a gradual approach to the design and build such a platform in 3 steps. The arrangement of stages will take into account the state of the available device technology and the trend in hardware and software integration design tools and the resources available for such a project. A conceptual diagram of the UMTS Terrestrial Radio Access Frequency Division Duplex (UTRA-FDD) transceiver with a channel simulator is proposed. Selected parts of this system will be designed, simulated and implemented progressively. The suggested block diagram applies for both up and downlink. **It can be also reconfigured to cope with the GSM, IS-136 and EDGE standards requirements.**

For this preliminary stage we consider a proposed design for SDR system that could be implemented in details subsequently through 3-4 projects for postgraduate students. This scheme establishes the necessary information to achieve the design stage in addition to a partial simulation results which pave the way to a complete simulator of SDR. It should reflect the main processing in the transmitter and receiver as well as different types of channel and multi-user effects.

The baseband signal processing of a software defined radio has to perform the following tasks (in the receiver):

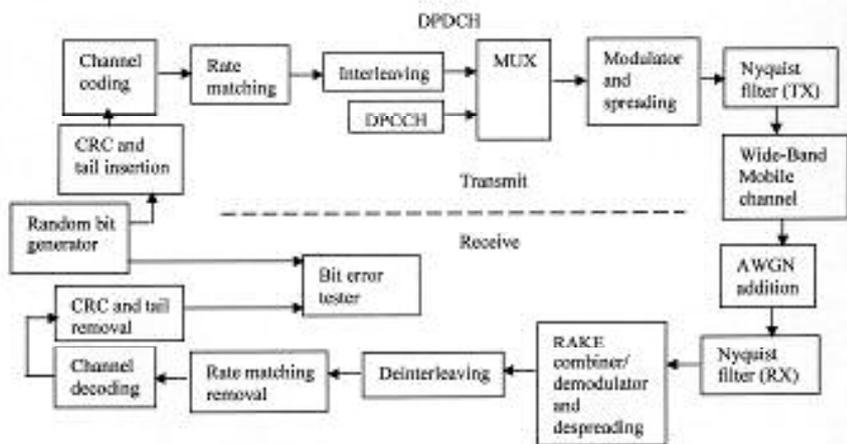
- Estimation of the channel impulse response
- Synchronisation
- Specific receiver algorithms like RAKE or multi-user detection
- Equalisation
- Demodulation
- Burst decomposition
- Channel decoding
- Source decoding

Herein, the most famous type of mobile phone standards are considered, i.e. WCDMA (UTRA-FDD), IS-136, GSM and EDGE. Other air-interface standards can be added after the success of this trial. More

emphasis will be given to the generalized modulator suggested into the transmitter stage of this system.

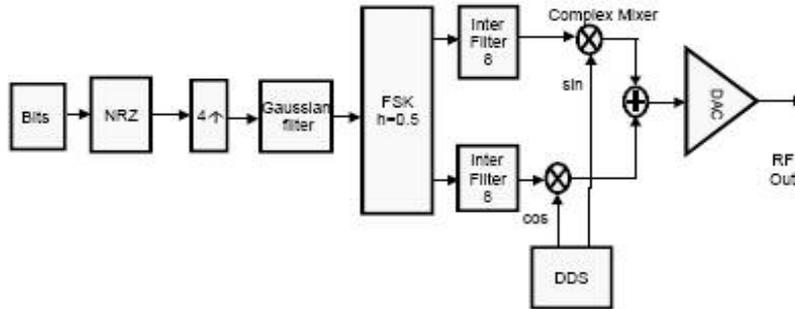
Based on the results reported on[2], the FPGA+DSP technology is suggested to be the most suitable available candidate for such work. Virtex XC2VP20 from Xilinx would be adopted in addition to TMS32060x from TI.

Figure (2) is a conceptual diagram of the UTRA-FDD transceiver in addition to a channel simulator with more emphasis on some parts of this system. The block diagram applies for both up and downlink.

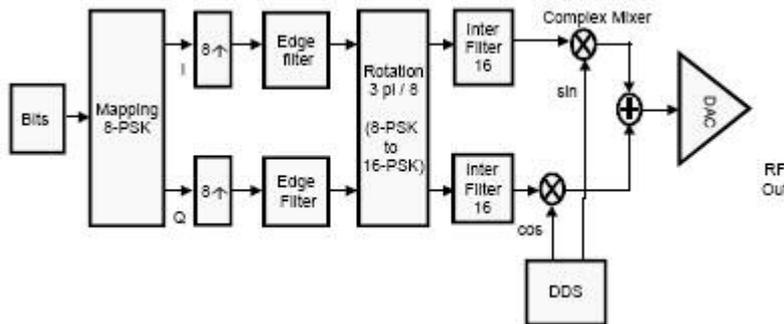


Figure(2):UTRA-FDD Transceiver + Channel Simulator

Figure (3) illustrate the block diagram of GSM system, while Figure(4) illustrate the EDGE transmitter system [6].



Figure(3): GSM transmitter



Figure(4): EDGE transmitter

4-1 Generalized Modulator

There are of course substantial differences between the 2nd generation standard (GSM, IS-136 ,EDGE) and the third generation standard (UMTS: UTRA-FDD). Our trial here is to design a reconfigurable scheme adaptable for all the selected systems. Starting with channel coding; we notice a little difference in the coding algorithms within the set of 2nd generation standards. For speech coding some combination of block coding for the most important speech bits and convolutional coding for the greater part of speech bits is applied. For data transmission a stronger convolutional coding is employed. UTRA-FDD offer higher data rates (up to 2Mbit/s) and should guarantee a BER of 10^{-6} for specific applications. Here, turbo codes are implemented which have to be integrated into general encoder and decoder structures. We will

concentrate here on the more interesting problem of general modulator structure.

According to Tables 2,3,4,5; UTRA-FDD, GSM, IS-136 and EDGE use QPSK, GMSK, $\pi/4$ -DQPSK and 8PSK respectively as modulation modes. Additionally, in UTRA-FDD the signal has to be spread to a chip rate of 3.84Mhip/sec. QPSK, $\pi/4$ -DQPSK and 8PSK are linear modulation modes while GMSK is nonlinear. Therefore we introduce a linearised version of GMSK to enable processing of both modulation scheme by a single generalized modulator into a SDR system[7]. Using a suitable linear approximation, GMSK signals can be produced by the same linear I/Q modulator employed for PSK signals. This is due to the fact that a GMSK signal may be pulse shaped with an impulse $C_0(t)$ that leads to a linear modulation . (The linear part contains about 99% of the signal energy.)

This generalized modulator structure is shown in Figure (5), taking into account that it can be extended to cope with UTRA-TDD, IS-136, GSM and EDGE signals.

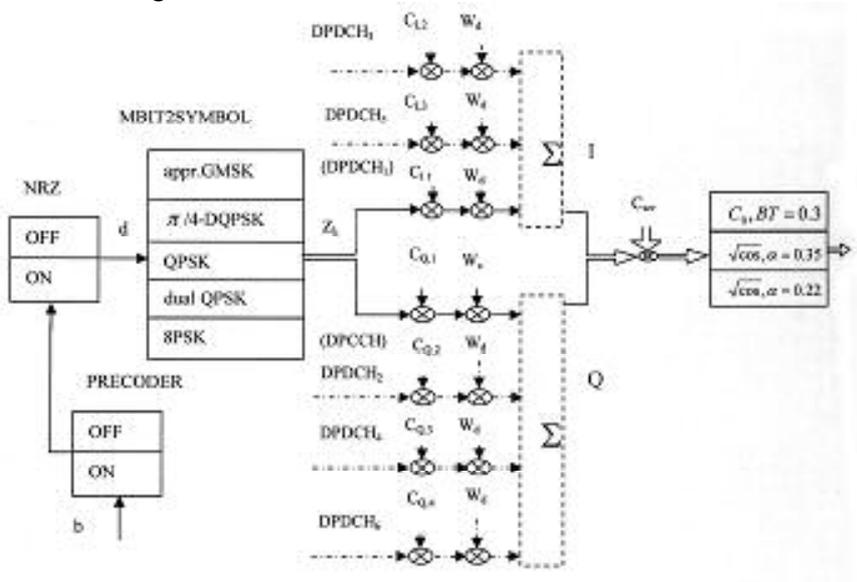


Figure 5: A Generalized Modulator for UTRA-FDD, GSM,IS-136, EDGE Systems

Differential precoding is necessary here for GSM and EDGE signal, where the bits $b_k \in \{0,1\}$; the precoding is defined by: $\beta_k = b_k + b_{k-1} \bmod 2$

The initialisation with $b_{-1} = 1$ results from the dummy bits which are sent in GSM before the first user bit during starting phase of a GSM and EDGE burst.

Two parameters control the switching of the precoding mainly: 'burst length' and 'precoder-on-off'. The parameter 'burst length' is used for the initialisation, while 'precoder-on-off' switches the power off if no GSM or EDGE signal to be handled.

The output of functional block (NRZ) is a non return to zero coded signal. For GSM signal this leads to $d_k = 1 - 2\beta_k$. This block is controlled by the parameter NRZ-on-off. If NRZ-on-off = 1, a bit $\beta = 0$ is transformed into $\beta' = 1$ and $\beta = 1$. For NRZ-on-off = -1 the reverse transformation results. NRZ-on-off = 0 indicates that no transform is performed.

In the next functional block, MBIT2 symbol, the bits are mapped to the complex symbol Z_k . The modulation mode is chosen by the parameter 'Modulation Number' whose function is as in Table 6:

Modulation Mode	Modulation Number
GMSK	1
$\pi/4$-DPSK	2
QPSK	3
Dual QPSK/8PSK	4

Table 6: Modulation Number for selected modulation schemes

An initial state has to be defined, since some modulation modes employ memory. Therefore the parameter 'burst length' is used in this block too. For UTRA-FDD uplink the control data of the DPDCH (dedicated physical data channel) are transmitted in the Q-branch and the information data of the first DPDCH are sent in the I-branch of DPDCH₁. This modulation may be interpreted as dual QPSK, where a serial to parallel transform is applied by directing I-length bits to the I-branch and Q-length bits to the Q-branch. The last two parameters are not used for GSM. Another option of UTRA-FDD is to switch more DPDCH onto the I- and Q-branches. These channels are indicated on Figure (5) in

dotted blocks since this option can only be chosen with a spread factor $N_s = 4$.

For UTRA-FDD, spreading is performed with the next processing step. This function is controlled by the parameter 'spreading factor'. The spreading sequences are stored and can be selected by the sequence number. For 'spreading factor' = 1, no spreading takes place. The following weighting of the data and control channels (DPDCH_i and DPCCH) with the weighting factors ω_d and ω_c , as well as the complex scrambling, is again performed only for UTRA-FDD.

(The next step is the complex impulse shaping, for which different finite impulse response FIR) filters can be employed by the parameter 'filter-number'; Table 7.

For GMSK the linear impulse $C_o(t)$ is used; for PSK modulations root raised cosine (RRC) roll off filters are applied.

Filter	Filter- Numbr
Main impulse $C_o(t)$ of linearised GMSK with BT= 0.3	1
Root raised cosine, roll-off factor $\alpha = 0.35$	2
Root raised cosine, roll-off factor $\alpha = 0.22$	3

Table 7: Pulse Shaping Filter Parameters

Table 8 represents the parameterisation of the general modulator required for GSM, IS-136, EDGE and UTRA-FDD. For UTRA-FDD the 'burst length' depends on the spreading factor. In this particular example we used 'spreading factor'-I = 8. For the DPCCH, on the other hand, 'spreading factor' - Q = 256 is always applied.

Parameter	GSM	IS-136	UTRA-FDD	EDGE
BurstLength (bits)	148	312	330	444
Precoder-On-Off	1	0	0	1
NRZ-On-Off	1	1	-1	1
ModulationNumber	1	2	4	4
Spreadingfactor-I	1	1	8	1
Spreadingfactor-Q	1	1	256	1
Filter-Number	1	2	3	1
I-length	-	-	320	-
Q-length	-	-	10	-

Table 8: Generalized Modulator, Parameterisation

4-2 SDR Receiver Implementation

The block diagram of the UTRA-FDD receiver is shown in Figure (6) as well as the transmitter. The received signal is first filtered by 49-tap RRC(Root-Raised Cosine) filter. The baseband signal is then fed into the Rake receiver, which has the task of despreading and demodulation, along with the correction for channel and transmitter impairments. The output of the Rake is then de-multiplexed to remove the various physical layer control information such as pilot and power control bits, and passed to the second interleaver [8].

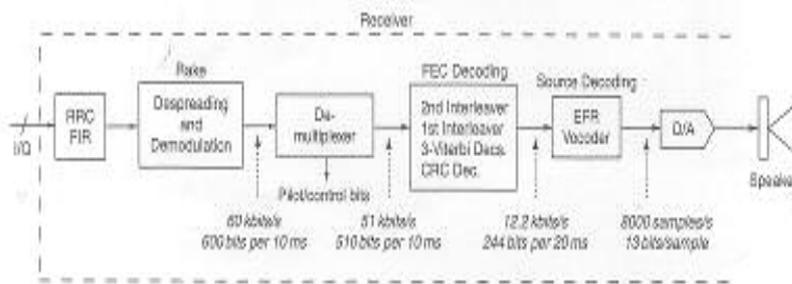


Figure (6): Preliminary SDR receiver

After collection of two radio frames, the first interleaving is performed on the received data, after which the DTX bits are removed. The received encoded bits are then processed by the 3 Viterbi decoders, for the 1/3 and 1/2 rate coders with a constraint length $K = 9$ (256 state Viterbi algorithm), to correct errors caused by the channel. CRC(Cyclic Redunency Check) parity decoding is performed on the RAB subflow No 1 (Radio Access Bearer) decoded bits to detect any uncorrected errors on this class of data. If CRC parity indicates an error, the 20ms speech frame is discarded, and the EFR vocoder is informed to repeat the last speech frame. If the CRC check does not detect any errors, the data stream is demultiplexed to its original state at 12.2 kb/sec. These bits are then processed by the GSM EFR decoder, to recover the original PCM speech frame at 104 kb/sec.

From the perspective of benchmarking, in terms of performance and bit-exact operation and algorithms, all the receiver blocks are well defined, with the exception of Rake receiver, where the computational load and

algorithmic complexity depend on the required performance, and can differ considerably for different implementations[9]. Since more than 70% of the total receiver processing power is consumed by the rake receiver block, it is important to discuss the operation and performance of this block further within a separate publication. We will manage to give more details later, about channel simulator and a couple of channel detectors.

Figure (7) illustrates the functional block diagram of GSM and EDGE receiver.

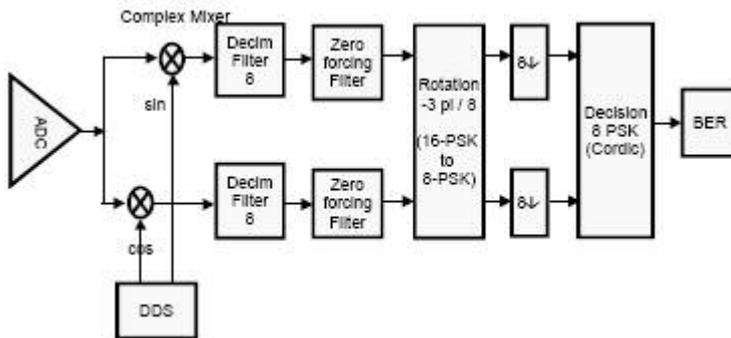


Figure (7-a):Block diagram of GSM receiver

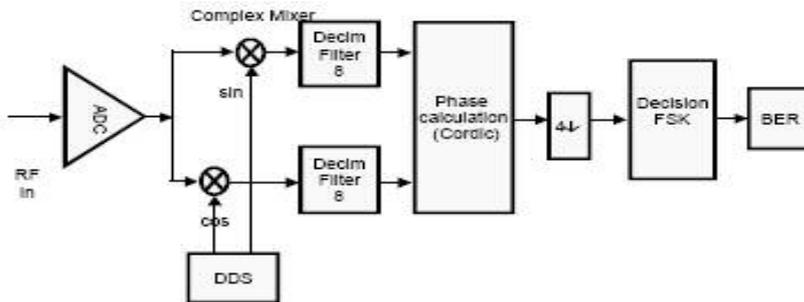


Figure (7-b): Block diagram of EDGE receiver

5- Results And Conclusions

Matlab simulation was used to develop the modules and to find the best values of parameters mentioned in the above paragraphs. The main achievement of our research work was the development of the generalized modulator so that it can perform the EDGE and IS-136 standards as well as the GSM and UTRA-FDD. This is considered as an important enlargement of the suggested SDR platform capabilities to be build in the Electronic and Computer Engineering department (ECE) at the University of Portsmouth.

In addition to that, a partial implementation of a rake receiver, based on FPGA and DSP devices, was also suggested and it will constitute the subject for future publication in collaboration with other researchers at the ECE – Portsmouth after the achievement of more simulation and testing.

We propose the following steps to build a physical complete SDR platform:

- 1- Adopting a hybrid solution of FPGA and DSP to build the general modulator and other constituents of the transmitter part.
- 2- Achieving the design and simulation stage of the rake receiver and other receiver components basing on the results of the conducted work.
- 3- Using Matlab, Simulink and RTL design tools is of high necessity to achieve the required design goals which are : optimal tasks assignment between the selected DSP and FPGA, maximum flexibility by reserving enough area on the FPGA for future updating, targeting low power consumption of the complete system.
- 4- Building the receiver section of the platform using FPGA+DSP according to the available funding.

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